IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer having a planar surface and oxide regions at said planar surface;

partially joining an integrated circuit wafer to [[a]] said supporting wafer at a limited number of joining points corresponding to said oxide regions;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

2. (Original) The method in claim 1, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

3. (Original) The method in claim 1, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points.

4. (Original) The method in claim 1, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

5. (Original) The method in claim 1, wherein said joining process comprises a bonding process.

6. (Original) The method in claim 1, wherein said joining process comprises a thermal oxide bonding process.

7. (Original) The method in claim 1, wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer.

8. (Currently Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer having a planar surface and oxide regions at said planar surface;

partially joining an integrated circuit wafer to [[a]] said supporting wafer at a limited number of joining points corresponding to said oxide regions;

reducing the thickness of said integrated circuit wafer;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

9. (Original) The method in claim 8, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

10. (Original) The method in claim 8, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points.

11. (Original) The method in claim 8, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

12. (Original) The method in claim 8, wherein said joining process comprises a bonding process.

13. (Original) The method in claim 8, wherein said joining process comprises a thermal oxide bonding process.

14. (Original) The method in claim 8, wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer.

15. (Currently Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer having a planar surface and oxide regions at said planar surface;

partially joining an integrated circuit wafer to [[a]] said supporting wafer at a limited number of joining points corresponding to said oxide regions;

chemically-mechanically polishing said integrated circuit wafer to reduce the thickness of said integrated circuit wafer;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

16. (Original) The method in claim 15, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

17. (Original) The method in claim 15, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points.

18. (Original) The method in claim 15, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

19. (Original) The method in claim 15, wherein said joining process comprises a bonding process.

20. (Original) The method in claim 15, wherein said joining process comprises a thermal oxide bonding process.